Please amend the present application as follows:

Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("——"), as is applicable:

1-16. (Canceled)

17. (New) A memory element comprising:

a top conductor;

a bottom conductor;

an isolator element disposed between the top conductor and the bottom conductor, the isolator element being formed of a high-resistance conductor; and

a non-conductive barrier layer disposed between the isolator element and the bottom conductor, the barrier layer being in contact with the bottom conductor;

wherein the bottom conductor and the barrier layer each comprise a non-uniform surface.

18. (New) The memory element of claim 17, wherein the memory element comprises an anti-fuse element.

19. (New) The memory device of claim 17, wherein an average thickness of the barrier layer is between 10 and 30 angstroms.

20. (New) The memory device of claim 17, wherein the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts.

21. (New) The memory element of claim 17, wherein the bottom conductor comprises a word line of a cross-point array of memory elements.

22. (New) The memory element of claim 21, wherein the barrier layer extends beyond the memory element along with the word line.

23. (New) The memory element of claim 17, wherein the bottom conductor is separate from a word line of a cross-point array of memory elements.

24. (New) A memory element comprising:

a top conductor;

a bottom conductor;

a silicon layer disposed between the top conductor and the bottom conductor; and

a non-conductive barrier layer disposed between the silicon layer and the top conductor, the barrier layer being in contact with the silicon layer;

wherein the silicon layer and the barrier layer each comprise a non-uniform surface.

25. (New) The memory element of claim 24, wherein the memory element comprises an anti-fuse element.

26. (New) The memory device of claim 24, wherein an average thickness of the barrier layer is between 10 and 30 angstroms.

27. (New) The memory device of claim 24, wherein the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts.

28. (New) The memory element of claim 24, wherein the silicon layer is in contact with the bottom conductor, the silicon layer and the bottom conductor together forming an isolator element comprising a schottky diode.

29. (New) A memory element comprising:

a top conductor;

a bottom conductor;

an isolator element disposed between the top conductor and the bottom conductor, the isolator element being formed as a p-n diode junction; and

a non-conductive barrier layer disposed between the isolator element and the bottom conductor, the barrier layer being in contact with the bottom conductor;

wherein the bottom conductor and the barrier layer each comprise a non-uniform surface.

30. (New) The memory element of claim 29, wherein the memory element comprises an anti-fuse element.

31. (New) The memory device of claim 29, wherein an average thickness of the barrier layer is between 10 and 30 angstroms.

32. (New) The memory device of claim 29, wherein the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts.

33. (New) The memory element of claim 29, wherein the bottom conductor comprises a word line of a cross-point array of memory elements.